REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-36 remain active in this application.

In the outstanding Office Action Claims 1-36 were rejected under 35 USC §102(b) as being anticipated by Saito et al.

Applicant respectfully traverses the outstanding rejection, because in Applicant's view, the pending claims patentably define over the applied prior art, for the reasons next discussed.

In particular, Saito et al. discloses a semiconductor memory device having a plurality of memory cells in an array, into which the memory cells data is writable, and which can subsequently be read. Each memory cell has a switching element with one terminal connected to a bit line of the array another terminal connected to at least one ferroelectric capacitor, and a control terminal connected to a word line. The cell may then be operated to detect the change in polarization of the ferroelectric capacitor when a voltage is applied which is not sufficient to cause a change of state of the ferroelectric capacitor.

Saito et al. in FIG. 4 discloses a plurality of ferroelectric capacitors 112-115 connected together at a common electrode and then connected to a bit line (BL) when MOS transistor 111 is turned on. The other ends of ferroelectric capacitors 112-115 are connected to respective plate lines 116, 117, 118 and 119. FIGS. 15 and 16 show a nothing but structure for uniting those ferroelectric capacitors.

The outstanding Office Action refers to column 18, line 62 to column 19, line 15, column 26, lines 13-23 and FIG. 21 of Saito et al. as teaching that a single ferroelectric capacitor has a plurality of polarization states to store multi-bit information.

However, in Saito et al., a memory of the multi-bit information utilizes a plurality of polarization states (P1, P2, P3, P3-, P2- and P1-) in hysteresis characteristics, as can be seen from FIG. 21. In practice, the polarized information is stored at different positions, and polarization states are reversed during reading, thereby to read electrical charge, and the read electrical charge is collected in an electrode provided at one side of the bit line BL.

In contrast, Applicant's invention is directed to a different phenomenon in which a specified atom has stabilized points with respect to other atoms at three or more positions in a two-dimensional plane of the perovskite structure that constitutes a ferroelectric film. That is, the polarization is held in the ferroelectric element at the same position.

On the contrary, Saito et al. does not teach that an electric field is applied to a single ferroelectric capacitor from a plurality of directions to find a plurality of stabilized positions therein, thereby storing a plurality of bit information.

In view of this clear distinction, it is respectfully submitted that pending Claims 1-36 clearly patentably distinguish over Saito et al, and are in condition for allowance. An early and favorable action to that effect is respectfully requested..

Respectfully submitted,

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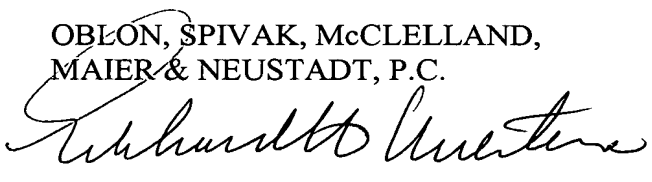

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